Application Note 51

Migrating from the TMC2490/TMC2491 to the TMC2490A/TMC2491A

The TMC2490A/TMC2491A is the latest encoder added to the Fairchild Semiconductor Division's roster of multimedia products. The TMC2490A/TMC2491A provides a number of feature enhancements over the existing TMC2490/ TMC2491.

Enhancements

- Macrovision 7.01 (TMC2491A only)
- 10 bit D/As
- Enhanced VBI controls

Modifications

- Synchronization signals
- Master mode operation.

Part Identification

The TMC2490A/TMC2491A can be identified by either the package marking or the control registers. The package marking for the TMC2490A/TMC2491A includes the letter 'A' for the part type. The previous marking was 2490R2C or 2491R2C, the new marking is now 2490AR2C or 2491AR2C. In addition, the revision identification is included at the end of the date code. The date code, yywwxxr, consists of the year (yy), week (ww), assembly site (xx), and revision (r). The revision id's for the TMC2490/TMC2491 are from 'A' to 'E' and for the TMC2490A/TMC2491A the revision id's are 'F' and greater. Two control registers have changed between the TMC2490/TMC2491 and the TMC2490A/TMC2491A that can be used to identify the A version from the non-A version. Part Identification register (0x00) has changed from a 0x94 to the new value for the TMC2490A/TMC2491A of 0x97. Also, if the Revision Identification register (0x03) contains a value greater than 0x04 this will identify the part as an 'A' version.

Macrovision 7.01 (TMC2491A only), 10 bit D/As, Enhanced VBI controls

With Macrovision 7.01 certification the TMC2490A/ TMC2491A is now DVD compliant and an ideal solution for PC-DVD applications. The new 10 bit D/As have improved the video performance of the TMC2490A/TMC2491A over the existing TMC2490/TMC2491. Luminance non-linearity, differential phase and differential gain have all been improved as the result of the 10 bit D/A. The VBI controls now include the ability to force a blanking level during the vertical blanking interval (VBI) in D1 mode and the ability to apply the same gain coefficients for active video lines with pedestal and no pedestal. The control register bits VBIEN (register 0x0F bit 3) and NGSEL (register 0x04 bit 6) control these functions.

Synchronization Signals

TMC2490/TMC2491

The generation of the synchronization signals (HSYNC, VSYNC, etc) in master mode is at the same time as what the TMC2490/TMC2491 generates in a D1 operation. The rising edge of PXCK that clocks in the C_B pixel data will generate the falling edge of HSYNC some n nanoseconds (specified by Tdo) after the rising edge of PXCK.

In the case of the TMC2490/TMC2491 Revision E, the generated HSYNC output in D1 and Master mode differs from the data sheet. In both modes of operation the falling edge of HSYNC is generated by the 43rd PXCK (Figure 1).

There are two outcomes of this timing. One, the 43rd PXCK will clock in an interpolated Y (luminance) pixel data. If a system is designed using the timing diagrams in the TMC2490 data sheet a C_B pixel data would be aligned with this clock. The result is a swapping of Y and C_B or C_R pixel data.

Two, since the HSYNC is generated later than expected a data shift occurs in the analog composite video. If a system is designed using the timing diagrams in the TMC2490 data sheet the active video pixels will be shifted to the left of the screen since we report the HSYNC later than expected.

TMC2490A/TMC2491A

The TMC2490A/TMC2491A corrects this problem and provides for multiple synchronization points. This allows the TMC2490A/TMC2491A to work with any decompression device. By configuring control register HDEL (0x0F bits 1-0) the position of HSYNC, relative to the PD port, can be aligned with either a C_B, C_R or Y data sample.

To match the HSYNC position of the TMC2490/TMC2491, relative to the C_B, Y C_R, Y_I data packet, a value of 0 needs to be placed in the HDEL control register. This will align the falling edge of HSYNC with the Y_I pixel data and the de-multiplexing of the pixel data will be the same as the non-A version of the TMC2490A/TMC2491A. However, there will be a shift in the output video position when it is compared to the TMC2490/TMC2491.

Master Mode Operation

TMC2490/TMC2491

In the TMC2490/TMC2491, the C_B, C_R demultiplexing is dependent on the state of CBSEL (internally referred to as PCKH). After $\overline{\text{RESET}}$ is toggled HIGH, the TMC2490/TMC2491's timing mode is configured to a D1 operation. If the TRS data packets are part of the pixel data, the correct C_B, C_R alignment, relative to HSYNC, occurs. When they are not present CBSEL simply keeps the state that it was initialized to and toggles at half the PCK rate.

When the master mode timing is configured two occurrences can happen. With TRS data packets inserted in the pixel data the correct C_B, C_R alignment relative to HSYNC occurs (Figure 3). This alignment is the result of the short period of time that the TMC2490/TMC2491 will operate in the D1 mode before switching to master mode. When TRS data packets are missing from the pixel data, the TMC2490/TMC2491 swaps the order of C_B and C_R relative to the HSYNC output (Figure 4). This is the result of CBSEL being initialized in the wrong state and not being correctly aligned with the HSYNC when TRS's are absent from the pixel data.

TMC2490A/TMC2491A

The TMC2490A/TMC2491A corrects this problem and always initializes the internal PCKH to the correct state as shown in Figure 3.

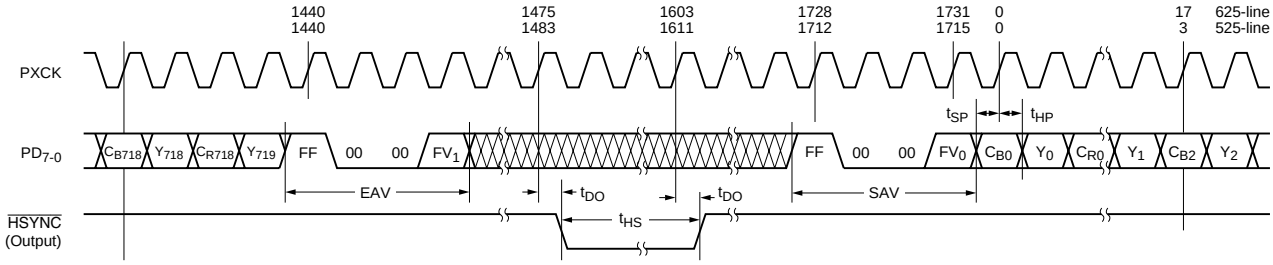

Figure 1. TMC2490/TMC2491 Revision E Timing

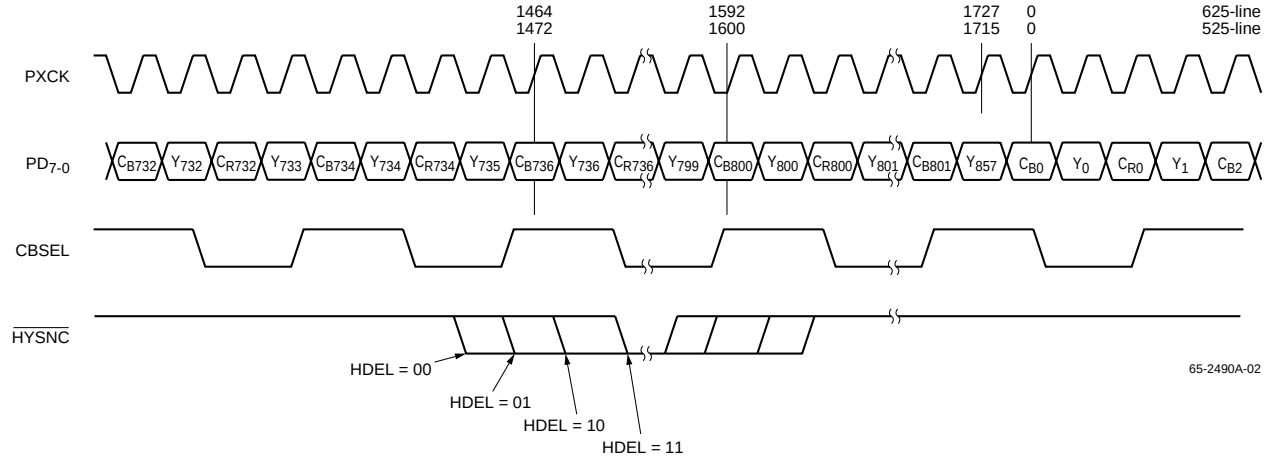

Figure 2. TMC2490A/TMC2491A Timing

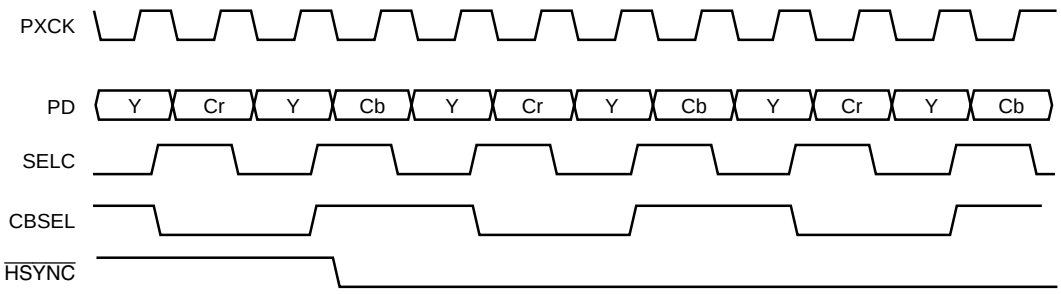

Figure 3. Master Mode Timing w/TRS in PD data

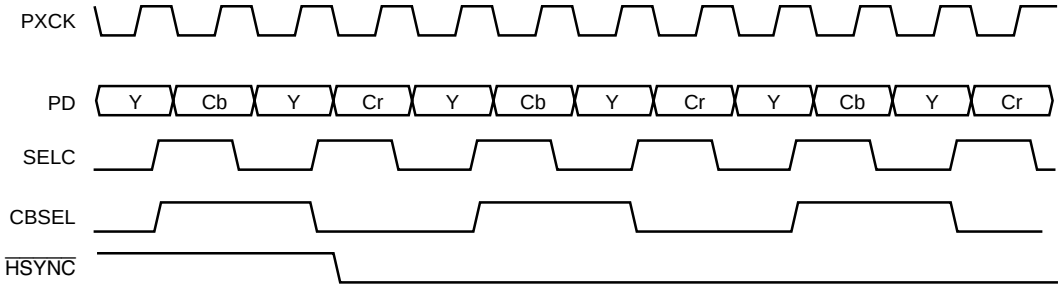

Figure 4. Master Mode Operation without TRS in PD data